UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,063	12/31/2001	Shrjie Tzeng	023925-00019	5645

32294 7590 11/18/2004

SQUIRE, SANDERS & DEMPSEY L.L.P.
14TH FLOOR
8000 TOWERS CRESCENT
TYSONS CORNER, VA 22182

EXAMINER	
IQBAL, NADEEM	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,063	TZENG, SHRJIE	
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "location determining unit", "fuse blowing unit", external processing unit" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 2 is objected to because of the following informalities: The word "first" in line 4, after "said" is misspelled as "fist". Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 7-24, 26-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al., (U.S. Patent number 6574763).

3. As per claims 1 & 20, Bertin et al., (Bertin) teaches (col. 2, lines 2-4) a memory array having redundant bits and addressable storage locations. He thus teaches limitations pertain to a buffer memory having a plurality of memory locations including redundant memory locations, memory locations having addresses. He also teaches (col. 2, lines 15-17) a test circuit adapted to couple to a memory array and generates test pattern and applies the test pattern to the memory array for testing. He thus teaches limitations pertain to a memory controller configured to read and write data. He also teaches (col. 7, lines 38-41) a control logic receives each address stored by the failed address buffer register, decodes failed address to a binary stream which correlates to a fuse string required to activate redundant element address steering (e.g. which fuses/antifuses must be blown). He thus teaches limitations pertain to plurality of fuses coupled to the memory controller. He also teaches (col. 5, lines 34-36) a test control circuit comprising a built-in-self-test circuit to determine an address of a failed memory location. He does not explicitly disclose a second plurality of fuses configured to store an address of a failed memory location. He teaches (col. 6, lines 28-30) a failed address buffer register that store the address of each memory

location having faulty bits. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to realize that his failed address buffer register performs equivalent function to that of second plurality of fuses, since it store the address of each memory location having faulty bits, and furthermore, he also teaches as stated above address steering and fuses/antifuses must be blown to activate the appropriate address redundancy, thus provides motivation for a person of ordinary skill in the art to utilize fuses to store an address of a failed memory location.

4. As per claims 2 & 21, Bertin already teaches as stated above a built-in-self-test circuit to determine an address of a failed memory location and address steering and that fuses/antifuses must be blown to activate the appropriate address redundancy, thus provides motivation for a person of ordinary skill in the art to utilize fuses to store an address of a failed memory location.

5. As per claims 3 & 22, Bertin teaches (col. 7, lines 44-47) a sparing control logic that activates the appropriate fuse strings and thereby enable the redundant elements to replace the failed bit in the memory array.

6. As per claims 4 & 23, Bertin teaches as stated per claim 2 above a built-in-self-test circuit to determine an address of a failed memory location and address steering and that fuses/antifuses must be blown to activate the appropriate address redundancy, thus provides motivation for a person of ordinary skill in the art to utilize fuses to store an address of a failed memory location.

7. As per claims 5 & 24, Bertin teaches (col. 7, lines 44-47) a sparing control logic that energizes the high voltage generators required to activates the appropriate fuse strings and thereby enable the redundant elements to replace the failed bit in the memory array.

8. Claims 6 & 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al., (U.S. Patent number 6574763) as applied to claim1-5 above, and further in view of Thomann et al., (U.S. Patent application number 2002/0169922).

9. Bertin does not explicitly disclose that the memory controller is configured to provide buffer pointers to the flow controller without using any failed memory locations based on data stored in the plurality of fuses. Thomann teaches (page 6, col. 1, lines 8-10) that if the address pad and fuse bank receives a memory address corresponding to a row address stored in the fuse bank, the address decoder is directed to select a redundant row rather than the row including the failed memory. It would have been obvious to a person of ordinary skill in the art to realize that Bertin would also include an address decoder to direct a redundant row rather than the row including the failed memory, since Bertin teaches also teaches (col. 7, lines 38-41) a control logic receives each address stored by the failed address buffer register, decodes failed address to a binary stream which correlates to a fuse string required to activate redundant element address steering, thereby includes logic to configure to use the redundant memory location instead of the failed memory location.

10. As per claims 7 & 26, Bertin teaches (col. 7, lines 44-47) a sparing control logic that energizes the high voltage generators required to activates the appropriate fuse strings and thereby enable the redundant elements to replace the failed bit in the memory array. He thus enables a bit for identifying if the fuse is enabled and a plurality of bits for storing an address of a failed memory location.

11. As per claims 8 & 27, Bertin teaches (col. 6, lines 28-30) a failed address buffer register that store the address of each memory location having faulty bits. He also teaches a built-in-self-test circuit to determine an address of a failed memory location as stated above.

12. As per claims 9 & 28, Bertin teaches (col. 3, lines 44,45) that a voltage may be written to each bit within the memory array and then read out to verify that the array is functioning. He thus teaches a SRAM.

13. As per claims 10 & 29, Bertin teaches (col. 7, lines 17-19) a controller 107 (Fig. 1) that issues a start command to the clocking control circuit. He thus teaches an external processing unit.

14. As per claims 11 & 30, Bertin teaches (col. 1, lines 22-24) that laser fuse blowing techniques improve device yield, and also teaches (col. 1, lines 33-35) electronic fuses and anifuses which may be electronically blown at the module level. He thus teaches external fuse blowing techniques.

15. As per claims 12 & 31, Bertin teaches (col. 7, lines 44,45) sparing control logic that energizes the high voltage generators required to activate the appropriate fuse strings. It would have been obvious to a person of ordinary skill in the art to realize that he would also utilize all of the first plurality of fuse means before using the second plurality of fuse means.

16. As per claim 13, Bertin et al., (Bertin) teaches (col. 2, lines 2-4) a memory array having redundant bits and addressable storage locations. He also teaches (col. 2, lines 15-17) a test circuit adapted to couple to a memory array and generates test pattern and applies the test pattern to the memory array for testing. He thus teaches limitations pertain to a testing a buffer memory having a plurality of memory locations and to determine if any of the locations are unusable. He

also teaches (col. 7, lines 38-41) a control logic receives each address stored by the failed address buffer register, decodes failed address to a binary stream which correlates to a fuse string required to activate redundant element address steering (e.g. which fuses/antifuses must be blown). He thus teaches limitations pertain to storing the address of the first unusable memory location. He also teaches (col. 5, lines 34-36) a test control circuit comprising a built-in-self-test circuit to determine an address of a failed memory location. He thus teaches to determine an address of a first unusable memory location. He does not explicitly disclose preventing a use of the first usable memory location based on the stored address of the unusable location. He teaches (col. 6, lines 28-30) a failed address buffer register that store the address of each memory location having faulty bits, and sparing control logic required to activate the appropriate fuse strings thereby enable the redundant elements to replace the failed bit in the memory array. It would have been obvious to a person of ordinary skill in the art he teaches to prevent a use of the unusable memory location based on the stored address, since he teaches sparing control logic required to activate the appropriate fuse strings thereby enable the redundant elements to replace the failed bit in the memory array, thereby preventing the use of the unusable memory location as claimed.

17. As per claim 14, He also teaches (col. 7, lines 38-41) a control logic receives each address stored by the failed address buffer register, decodes failed address to a binary stream which correlates to a fuse string required to activate redundant element address steering (e.g. which fuses/antifuses must be blown). He thus teaches limitations pertain to storing the address of the second unusable memory location in a fuse of the first plurality of fuses. He also teaches (col. 5, lines 34-36) a test control circuit comprising a built-in-self-test circuit to determine an

address of a failed memory location. He thus teaches to determine an address of a second unusable memory location.

18. As per claim 15, He also teaches (col. 2, lines 15-17) a test circuit adapted to couple to a memory array and generates test pattern and applies the test pattern to the memory array for testing. He also teaches (col. 5, lines 34-36) a test control circuit comprising a built-in-self-test circuit to determine an address of a failed memory location. He thus teaches limitations pertain to testing a buffer memory comprising a built-in test.

19. As per claims 16 & 17, He also teaches (col. 5, lines 34-36) a test control circuit comprising a built-in-self-test circuit to determine an address of a failed memory location. He thus teaches to determine addresses of unusable memory locations.

20. As per claim 18, He does not explicitly disclose a second plurality of fuses configured to store an address of a failed memory location. He teaches (col. 6, lines 28-30) a failed address buffer register that store the address of each memory location having faulty bits. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to realize that his failed address buffer register performs equivalent function to that of second plurality of fuses, since it store the address of each memory location having faulty bits, and furthermore, he also teaches as stated above address steering and fuses/antifuses must be blown to activate the appropriate address redundancy, thus provides motivation for a person of ordinary skill in the art to utilize fuses to store an address of a failed memory location.

21. As per claim 19, He teaches (col. 2, lines 15-17) a test circuit adapted to couple to a memory array and generates test pattern and applies the test pattern to the memory array for testing. He also teaches (col. 5, lines 34-36) a test control circuit comprising a built-in-self-test

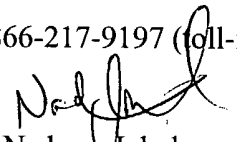
circuit to determine an address of a failed memory location. He thus teaches limitations pertain to testing a buffer memory.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (571)-272-3659. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571)-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Nadeem Iqbal
Primary Examiner
Art Unit 2114

NI